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EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2827	2

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/858,238	Applicant(s) CHONG ET AL.
	Examiner John B. Vigushin	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-23 and 25-35* is/are rejected.

7)☒ Claim(s) *6 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 13-15 are objected to because of the following informalities:

a) Claim 13, line 1: before "least" insert --at--.

b) Claims 14 and 15 depend from Claim 13 and therefore inherit the defect of that claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 2, 8, 20, 28 and 33 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for determining the maximum trace escape density (TED), does not reasonably provide enablement for determining the maximum land density. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Page 14, lines 15-25 of the Specification clearly teaches that **the maximum trace escape density** (*not* the land density) equals the reciprocal of (Tw + Ts), where Tw is the width of the substrate traces and Ts is the spacing between the substrate traces. There is no support in the

Specification that the reciprocal of (Tw + Ts) determines the **density of the lands** as recited in the above-cited claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1-5, 19-23 and 25-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Horiuchi et al.

As to Claim 1, Horiuchi et al. discloses: a substrate on which to mount an IC having a first dense formation of lands (col.2: 27-35); a second dense formation of lands on a surface thereof formed in a geometrical pattern to maximize the density of the second dense formation of lands (col.11: 22-30; col.9: 38-52), while constrained by the size of the individual lands and by the width and spacing of substrate traces coupled to the lands (Figs. 12 to 17; col.5: formulae at lines 55 and 61; col.10: 40-63).

As to Claims 2 and 20 (as best understood by the Examiner in view of the above 35 USC § 112, 1st paragraph rejection), Horiuchi et al. does not explicitly compute the maximum trace escape density (TED) for the given configuration of the second dense

formation of lands (col.9: 38-52) but *inherently*, the maximum TED for the above-disclosed land configuration given by Horiuchi et al. is the reciprocal of the sum of the routing line width Tw and the space Ts between the routing lines, i.e., Tw + Ts (support for this inherent property is found in the denominator of the formula at col.5, line 55). For example, using the data provided for the exemplary application in Figs. 12-17, Ts = Tw = 50μm (col.10: the Table at line 50 and the statement at line 53). Therefore, $TED_{max} = 1/(Ts + Tw) = 1/(50\mu m + 50\mu m) = 1/100\mu m$ = 10 routing lines per millimeter.

As to Claims 3 and 21, Horiuchi et al. further discloses that the second dense formation of lands is formed as a plurality of zigzag rows (Figs. 7-10 and 12-17).

As to Claims 4 and 22, Horiuchi et al. further discloses that the second dense formation of lands is formed as a plurality of zigzag rows and these rows are substantially parallel (Figs. 12-17; col.10: 64-65).

As to Claims 5 and 23, Horiuchi et al. further discloses that the second dense formation of lands is formed in a zigzag pattern (Fig. 7 and Figs. 12-17).

As to Claim 19, Horiuchi et al. discloses: forming on a substrate surface a plurality of traces (Figs. 7-10 and 12), the traces having at least a predetermined width and a predetermined spacing from one another (col.5: the formula at line 55; col.10: the Table at line 50 and the statement at line 53); forming on the substrate surface a plurality of lands, each coupled to a corresponding one of the traces (Figs. 7, 9,10 and 12), and each having at least a predetermined size (col.5: the formula at line 55; col.10: the Table at line 50), the plurality of lands being formed in a geometrical pattern that maximizes the density of such lands (col.11: 22-30; col.9: 38-52) while constrained by

the land size and by the width and spacing of the traces (Fig. 12; col.5: formulae at lines 55 and 61: col.10: 40-63).

As to Claim 25, Horiuchi et al. discloses: for a first layer (Fig. 12), forming a first plurality of traces having at least a predetermined width and a predetermined spacing from one another; for a second layer (Fig. 13), forming a second plurality of traces having at least a predetermined width and a predetermined spacing from one another (col.10: 40-53); for the first and second layers, forming a plurality of vias to couple ones of the first plurality of traces to ones of the second plurality of traces (col.3: 53-62; col.11: 32-43); for the second layer (Fig. 13) forming a plurality of lands each coupled to a corresponding one of the plurality of traces of the second layer, and each having at least a predetermined size (col.5: the formula at line 55; col.10: the Table at line 50), the first plurality of lands being formed in a geometrical pattern that maximizes the density of the first plurality of lands (col.11: 22-30; col.9: 38-52) while constrained by the land size and by the width and spacing of the traces of the second layer (Fig. 13; col.5: formulae at lines 55 and 61: col.10: 40-53).

As to Claim 26, each via inherently has at least a predetermined size and Horiuchi et al. further discloses for the second layer, forming a second plurality of lands (Fig. 13) each coupled through a corresponding via to a corresponding one of the plurality of traces of the first layer (col.3: 53-62; col.11: 32-43), the plurality of lands being formed in a geometrical pattern that maximizes the density of the second plurality of lands (Figs. 13; col.11: 22-30; col.9: 38-52) while constrained by the width and

spacing of the traces of the first layer (Fig. 12; col.5: formulae at lines 55 and 61; col.10: 40-53).

As to Claim 27, the second plurality of lands is formed in a geometrical pattern that maximizes the density of the second plurality of lands while additionally constrained by the via size which is inherently the case since the land density directly depends on the via size as shown in Fig. 20.

As to Claim 28 (as best understood by the Examiner in view of the above 35 USC § 112, 1st paragraph rejection), Horiuchi et al. does not explicitly compute the maximum trace escape density (TED) for the given configuration of the first plurality of lands (col.9: 38-52) but *inherently*, the maximum TED for the above-disclosed land configuration given by Horiuchi et al. is the reciprocal of the sum of the routing line width Tw and the space Ts between the routing lines, i.e., Tw + Ts (support for this inherent property is found in the denominator of the formula at col.5, line 55). For example, using the data provided for the exemplary application in Figs. 12-17, Ts = Tw = 50μm (col.10: the Table at line 50 and the statement at line 53). Therefore, $TED_{max} = 1/(Ts + Tw) = 1/(50\mu m + 50\mu m) = 1/100\mu m$ = 10 routing lines per millimeter.

As to Claim 29, Horiuchi et al. further discloses that the first plurality of lands is formed as a plurality of zigzag rows (Figs. 7-10 and 12-17).

As to Claim 30, Horiuchi et al. further discloses that the plurality of zigzag rows are substantially parallel (Figs. 12-17; col.10: 64-65).

As to Claim 31, Horiuchi et al. further discloses that the second dense formation of lands is formed in a zigzag pattern (Fig. 7 and Figs. 12-17).

As to Claim 32, Horiuchi et al. discloses forming lands on a substrate surface in a geometrical pattern to maximize the density of such lands while constrained by the land size and by the width and spacing of traces coupled to the lands and formed on the substrate surface (Figs. 7-10 and 12; col.11: 22-30; col.9: 38-52; col.5: formulae at lines 55 and 61; col.10: 40-63); coupling lands on an IC to corresponding lands on the substrate surface (Fig. 20; col.2: 27-31; col.10: 40-44).

As to Claim 33 (as best understood by the Examiner in view of the above 35 USC § 112, 1st paragraph rejection), Horiuchi et al. does not explicitly compute the maximum trace escape density (TED) for the given configuration of the second dense formation of lands (col.9: 38-52) but *inherently*, the maximum TED for the above-disclosed land configuration given by Horiuchi et al. is the reciprocal of the sum of the routing line width Tw and the space Ts between the routing lines, i.e., Tw + Ts (support for this inherent property is found in the denominator of the formula at col.5, line 55). For example, using the data provided for the exemplary application in Figs. 12-17, Ts = Tw = 50μm (col.10: the Table at line 50 and the statement at line 53). Therefore, $TED_{max} = 1/(Ts + Tw) = 1/(50\mu m + 50\mu m) = 1/100\mu m = 10$ routing lines per millimeter.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7-15, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. in view of Akram et al.

As to Claims 7 and 13:

I. Horiuchi et al. discloses an IC comprising a first plurality of lands on a surface thereof, including a first dense formation of lands (col.2: 27-31; col.10: 40-44); a substrate comprising a second plurality of lands on a surface thereof, including a second dense formation formed in a geometrical pattern to maximize the density of the second dense formation of lands (col.11: 22-30; col.9: 38-52), while constrained by the size of the second dense formation of lands and by the width and spacing of substrate traces coupled to the second dense formation of lands (Figs. 12 to 17; col.5: formulae at lines 55 and 61; col.10: 40-63).

II. Horiuchi et al. is silent as to elements coupling the first plurality of lands to the second plurality of lands.

III. Akram et al. discloses lands 28 of IC 24 coupled to lands 44 of substrate 16 by (solder) elements 50 as is well-known in the art (Fig. 2; col.11: 7-9).

IV. Since both Horiuchi et al. and Akram et al. are both in the electronics packaging art, the use of solder elements for coupling the lands of an IC to the lands of a substrate taught by Akram et al. would have been readily recognized in the pertinent art of Horiuchi et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize solder elements in Horiuchi et al. to couple

the dense formation of IC lands to the dense formation of substrate lands, as taught by Akram et al.

As to Claim 8 (as best understood by the Examiner in view of the above 35 USC § 112, 1st paragraph rejection), modified Horiuchi et al. does not explicitly compute the maximum trace escape density (TED) for the given configuration of the second dense formation of lands (col.9: 38-52) but *inherently*, the maximum TED for the above-disclosed land configuration given by Horiuchi et al. is the reciprocal of the sum of the routing line width Tw and the space Ts between the routing lines, i.e., Tw + Ts (support for this inherent property is found in the denominator of the formula at col.5, line 55). For example, using the data provided for the exemplary application in Figs. 12-17, Ts = Tw = 50μm (col.10: the Table at line 50 and the statement at line 53). Therefore, $TED_{max} = 1/(Ts + Tw) = 1/(50μm + 50μm) = 1/100μm$ = 10 routing lines per millimeter.

As to Claim 9, modified Horiuchi et al. further discloses that the second dense formation of lands is formed as a plurality of zigzag rows at the periphery of the surface of the substrate (Figs. 7-10 and 12).

As to Claims 10 and 14, modified Horiuchi et al. further discloses that the second dense formation of lands is formed in a zigzag pattern (Fig. 7 and Figs. 12-17).

As to Claims 11, 12, 15, 34 and 35:

I. Horiuchi et al. discloses that the IC may be a semiconductor chip or device (col.2: 27-29), wherein a "chip" is often interpreted in the art as a bare die, and a "device" is often interpreted in the art as a packaged die.

II. Akram et al. explicitly indicates that IC 24 may be either a bare die or a packaged die (col.9: 43-49).

III. Since both Horiuchi et al. and Akram et al. are both in the electronics packaging art, the use of either a bare (i.e., unpackaged) die or a packaged die, as taught by Akram et al., would have been readily recognized in the pertinent art of Horiuchi et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use either a unpackaged (bare) die (IC "chip") or a packaged die (IC "device") in electronic assembly of Horiuchi et al. in order to meet the performance requirements of the electronic assembly, as taught by Akram et al.

8. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. in view of Akram et al. and Bothra et al.

As to Claim 16:

I. Horiuchi et al. discloses an IC comprising a first plurality of lands on a surface thereof, including a first dense formation of lands (col.2: 27-31; col.10: 40-44); a substrate comprising a second plurality of lands on a surface thereof, including a second dense formation formed in a geometrical pattern to maximize the density of the second dense formation of lands (col.11: 22-30; col.9: 38-52), while constrained by the size of the second dense formation of lands and by the width and spacing of substrate traces coupled to the second dense formation of lands (Figs. 12 to 17; col.5: formulae at lines 55 and 61; col.10: 40-63).

IIa. Horiuchi et al. is silent as to elements coupling the first plurality of lands to the second plurality of lands.

IIb. Akram et al. discloses lands 28 of IC 24 coupled to lands 44 of substrate 16 by (solder) elements 50 as is well-known in the art (Fig. 2; col.11: 7-9).

IIc. Since both Horiuchi et al. and Akram et al. are both in the electronics packaging art, the use of solder elements for coupling the lands of an IC to the lands of a substrate taught by Akram et al. would have been readily recognized in the pertinent art of Horiuchi et al.

IId. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize solder elements in Horiuchi et al. to couple the dense formation of IC lands to the dense formation of substrate lands, as taught by Akram et al.

III. Horiuchi et al. does not teach : a data processing system to which the electronic assembly of Horiuchi et al. is applied, wherein: a bus couples components in the data processing system, a display, an external memory and a processor are coupled to the bus, said processor including at least one electronic package comprising the claimed structural elements recited in part I, above.

IVa. Bothra et al. discloses a data processing system 800 in Fig. 8 (col.10: 39-52) wherein a bus 824 couples components 804, 806, 808, 810 and 812 in the data processing system; a display 804 coupled to bus 824; an external memory 808 (floppy disk drive) coupled to bus 824; and a processor 816 coupled to the bus and

including an electronic package 200 (i.e., the disclosed invention in Fig. 4A) or the prior art package 100 in Fig. 1A (col.1: 43-56).

IVb. Since both Bothra et al. and Horiuchi et al. are in the electronics packaging art and disclose a semiconductor device package, and Bothra et al. applies the semiconductor device package (functionally, a microprocessor) in the above-described data processing system, then the analogous application of the structurally enhanced semiconductor package of Horiuchi et al., designed to function as a microprocessor, to a data processing system, as taught in Bothra et al. would have been readily recognized by and obvious to one of ordinary skill in the pertinent electronics packaging art of Horiuchi et al.

As to Claim 17, Horiuchi et al. further discloses that the second dense formation of lands is formed in a zigzag pattern (Fig. 7 and Figs. 12-17).

9. Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi et al. in view of Akram et al. and Bothra et al., as applied to claim 16 above, and further in view of Bertin et al.

I. Modified Horiuchi et al. discloses that the IC may be a semiconductor chip or device (col.2: 27-29), wherein a "chip" is often interpreted in the art as a bare die, and a "device" is often interpreted in the art as a packaged die.

II. Bertin et al. explicitly teaches that a processor (CPU) can either a packaged die 97′ (Fig. 5(a)(2)) or an unpackaged die 97″ (Fig. 5b and col.9: 14-16).

III. Since both modified Horiuchi et al. and Bertin et al. are both in the electronics packaging art, a processor including either a bare (i.e., unpackaged) die or a packaged

die, as taught by Bertin et al., would have been readily recognized in the pertinent art of Horiuchi et al. as modified by Bothra et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use either an unpackaged (bare) die (IC "chip") or a packaged die (IC "device") as the semiconductor processor device in the electronic assembly of modified Horiuchi et al. in order to meet the performance requirements of the processor device in the data processing system, as taught in Horiuchi et al. as modified by Bothra et al.

Allowable Subject Matter

10. Claims 6 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 6 and 24, patentability resides in that the lands are formed in a pattern comprising *a combination of a face center rectangular pattern and a pattern form the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of a zigzag pattern, a wave pattern, an undulating pattern, and a vertical stack pattern*, in combination with the other limitations of Claims 6 and 24, respectively.

12. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Horiuchi et al. (US 6,194,668 B1 and US 6,271,478 B1) discloses a multilayer circuit board with wiring pattern that reduces the required number of wiring layers by enhancing the trace density on each layer (see US 6,194,668 B1: col.2: 54-col.3: 3; and US 6,271,478 B1: col.2: 16-29).

b) Ghahghahi (US 6,150,729) discloses a circuit board having a wiring arrangement that enhances the trace density on a surface of the circuit board (Fig. 3b; col.2: 64-col.3: 14).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin

John B. Vigushin
Examiner
Art Unit 2827

jbv
July 11, 2002